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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TOLEDO, FERNANDO L	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,580	FUJITA, HARUMITSU	
	Examiner	Art Unit	
	Fernando L. Toledo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/021,519.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 20 rejected under 35 U.S.C. 102(b) as being anticipated by Hidaka (U. S. patent 5,668,755 A).

Hidaka discloses in the U. S. patent 5,668,755 A; figures 1 – 55 and related text, (a) doping a high voltage CMOS circuit at a low impurity concentration; and (b) doping a low voltage CMOS circuit at a high impurity concentration after the step (a) (Column 8, lines 15 – 67).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9 – 15, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka in view of Mogami et al. (U. S. patent 5,571,735 A).

In re claim 9, Hidaka discloses (a) providing a semiconductor substrate 1 having at least first and second active regions (12 and 16) of a first conductivity type and at least third and fourth active regions (13 and 14) of a second conductivity type; (b) forming a gate oxide layer having a first thickness onto at least the first, second, third and fourth active regions (Column 8, lines 26 and 27); (c) forming an electrode layer onto said gate oxide layer (22, 23, 24 and 26); (d) patterning the electrode layer to form first, second, third and fourth gate electrodes (22, 23, 24 and 26) onto the first, second, third and fourth active regions respectively; (e) doping the first active region and the first gate electrode with an impurity of the second conductivity type to form a first transistor driven at a first voltage level, the first gate electrode being doped at a first concentration (Column 8, lines 38 – 50); (f) doping the second active region and the second gate electrode with an impurity of the second conductivity type to form a second transistor to be driven at a second voltage level lower than the first voltage level, the second gate electrode being doped at a first concentration (Column 8, lines 38 – 50); (g) doping the third active region and the third gate electrode with an impurity of the first conductivity type to form a third transistor to be driven at the first voltage level, the third gate electrode being doped at a third concentration (Column 8, lines 38 – 50); (h) doping the fourth active region and the fourth gate electrode with an impurity of the first conductivity type to form a fourth transistor to be driven at the second voltage level, the fourth gate electrode being doped at a fourth concentration (Column 8, lines 38 – 50).

Hidaka does not teach wherein the electrode layer is formed of undoped polysilicon. However, Mogami in the U. S. patent 5,571,735 A; figures 1A – 8D and related text discloses

forming CMOS gate transistor with undoped polysilicon as an alternate way to form gate transistors for a CMOS device (Column 9, lines 11 – 15).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Hidaka and Mogami to enable forming the gate electrodes of Hidaka to be performed according to the teachings of Mogami by forming the gate electrodes of undoped polysilicon because one of ordinary skill in the art would have been motivated to look to alternative suitable methods of performing forming the gate electrodes of Hidaka and art recognized suitability for an intended purpose has been recognized to be motivation to combine. See MPEP §2144.07.

5. In re claim 10, Hidaka discloses wherein the doping steps (e) to (h) includes implanting ions of an impurity in the active regions and the gate electrodes (Column 8, lines 27 – 30).

6. In re claim 11, Hidaka discloses wherein the lower concentration of impurities in the first and third gate electrodes causes the creation of a depletion layer in the first and third gate electrodes when a driving voltage is applied thereto (Column 8, lines 38 – 50).

7. In re claim 12, Hidaka discloses wherein the first active region and the first gate electrode are doped simultaneously (Column 8, lines 27 – 30).

8. In re claim 13, Hidaka discloses wherein the second active region and the second gate electrode are doped simultaneously (Column 8, lines 27 – 30).

9. In re claim 14, Hidaka discloses wherein the third active region and the third gate electrode are doped simultaneously (Column 8, lines 27 – 30).

10. In re claim 15, Hidaka discloses wherein all of the gate oxides have the same thickness (Column 8, lines 26 – 27).

11. In re claim 19, Hidaka discloses wherein the depletion region in the gate electrode makes a dielectric breakdown voltage between the gate electrode and the active region higher (Column 8, lines 36 – 50).

12. In re claim 22, Hidaka discloses wherein the fourth active region and the fourth gate electrode are doped simultaneously (Column 8, lines 27 – 30).

13. Claims 16 – 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka in view of Mogami as applied to claims 9 – 15, 19, 20 and 22 above, and further in view of Tigelaar et al. (U. S. patent 5,595,922).

In re claim 16, Hidaka in view of Mogami does not show wherein all of the gate oxides have a shape wherein they are thicker at side edges of the gate electrodes than at the center thereof.

However, Tigelaar in the U. S. patent 5,595,922; figures 1 – 5 and related text, discloses wherein all of the gate oxides have a shape wherein they are thicker at side edges of the gate electrodes than at the center thereof since they seal the gate structure so as to reduce any electrical leakage from the gate structure (column 3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate oxide of Hidaka in view of Mogami wherein all of the gate oxides have a shape wherein they are thicker at side edges of the gate electrodes than at the center thereof, as taught by Tigelaar, since they seal the gate structure so as to reduce any electrical leakage from the gate structure.

14. In re claims 17 and 21, Hidaka in view of Mogami does not show further including oxidizing the side walls of the gate electrodes, the gate oxides under each of the gate electrode being thickened at the edge portions while the sidewalls are oxidized.

Tigelaar discloses oxidizing the side walls of the gate electrodes, the gate oxides under each of the gate electrode being thicker at the edge portions while the sidewalls are oxidized, since they seal the gate structure so as to reduce any electrical leakage from the gate structure (column 3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate oxide of Hidaka in view of Mogami oxidizing the side walls of the gate electrodes, the gate oxides under each of the gate electrode being thicker at the edge portions while the sidewalls are oxidized, as taught by Tigelaar, since they seal the gate structure so as to reduce any electrical leakage from the gate structure.

15. In re claim 18, Hidaka in view of Mogami does not show further including oxidizing the first and second gate electrodes to form an oxide film under the gate electrodes, the oxide film being thicker at an edge portion than at the center portion of the gate electrodes.

Tigelaar discloses oxidizing the first and second gate electrodes to form an oxide film under the gate electrodes, the oxide film being thicker at an edge portion than at the center portion of the gate electrodes, since they seal the gate structure so as to reduce any electrical leakage from the gate structure (column 3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate oxide of Hidaka in view of Mogami oxidizing the first and second gate electrodes to form an oxide film under the gate electrodes, the oxide film being

thicker at an edge portion than at the center portion of the gate electrodes, as taught by Tigelaar, since they seal the gate structure so as to reduce any electrical leakage from the gate structure.

Response to Arguments

16. Applicant's arguments filed 23 December 2004 have been fully considered but they are not persuasive for the following reasons.

17. Applicant argues that Hidaka does not show doping at high and low concentrations the source and drain regions. However, in order to make a memory device having a memory region and a peripheral region it is imperative to have a low voltage (i.e. low impurity concentration) region and a high voltage (i.e. high impurity concentration) region. This is stated in the prior art particularly in the abstract of U. S. Patent 5,396,098 belonging to Kim et al. This statement in no way changes the rejection but merely clears the point that although Hidaka does not explicitly shows a particular limitation (namely the high and low impurity concentration), it is an implicit limitation that Hidaka possess, since the device of Hidaka has a memory region and a peripheral region.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Thu 7am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Fourson
Primary Examiner
Art Unit 2823

FToledo
15 March 2005